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Design of 16-Bit Carry Select Adder with Low Power 8-Transistor Full Adder Cell

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Abstract **- An addition is a fundamental arithmetic operation which is used extensively in many very large-scale integration (VLSI) chips such as application-specific digital signal processing (DSP) and microprocessors chips. An adder determines the overall performance of the circuits in most of those systems. Carry select adder (CSLA) is one of the fastest adders used in many data processing processors to perform fast arithmetic functions of n-bit additions when compared with ripple carry adders. From the structure of the CSLA, it is clear that there is a scope for reducing the area and power consumption in the CSLA.This work uses simple and efficient transistor level modifications to significantly reduce the area and power of the CSLA.Based on these modifications in this paper 16-bit CSLA architecture have been developed and compared with the regular CSLA architecture. The proposed design has reduced area and power as compared with the regular CSLA with only a slight increase in the delay. This work evaluates the performance of the proposed designs in terms of delay, area, power, and their products by hand with logical effort and through custom design and layout in 0.18-µm CMOS process technology. The results analysis shows that the proposed CSLA structure is better than the regular CSLA.**

Keywords **- CSLA, Full Adder, Multiplexer, Very Large-Scale Integration (VLSI).**

I. INTRODUCTION

Adder is one of the most widely used building blocks in all data processing (arithmetic) and digital signal processing architectures. Addition usually impacts widely on the overall performance of digital systems. In VLSI applications, area and power are very important factors that are taken into account while designing fast adders [1]. Every aspect of the adder design directly relates to area optimization. The carry-ripple adder is composed of many cascaded single-bit full-adders as shown in figure 1. Concatenating the n full adders forms n-bit ripple carry adder. The circuit architecture is simple and area-efficient. However, the computation speed is slow [1] because each full-adder can only start operation till the previous carry-out signal is ready. In the carry select adder (CSLA), n bits adder is divided into m parts. each part of adder is composed two carry ripple adders with Cin=0 and Cin=1, respectively. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of ripple carry adders (RCA) to generate partial sum and carry by considering carry input Cin = 0 and Cin = 1, then the final sum and carry are selected by the multiplexers.

In this paper eight transistor 1-bit full adder used for each full adder block in first RCA block with Cin = 0, 2-transistor multiplexer and a binary to excess-1 converter (BEC) used instead of RCA block with Cin = 1 in the regular CSLA to achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit ripple adder (RCA) structure [2],[3] & [5].A novel eight transistor 1-bit full adder used for each full adder block because of its less transistor count & less power-delay product[4].

This paper is organized as follows, in section 2, we examine the conventional carry select adder, in section 3 we look at the architecture of the proposed carry select adder, in section 4 result analysis are discussed. The section 5 was ended with conclusion.

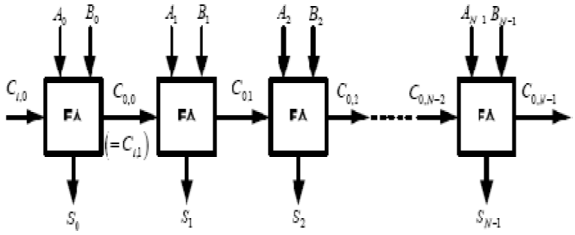

Fig.1. N-Bit Carry Ripple Adder Constructed By N Single Bit Full-Adders

II. REGULAR CARRY SELECT ADDER

The carry-select adder generally consists of two ripple carry adders and a multiplexer as shown in figure 2. Adding two n-bit numbers with a carry-select adder is done with two adders (two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry input is known.

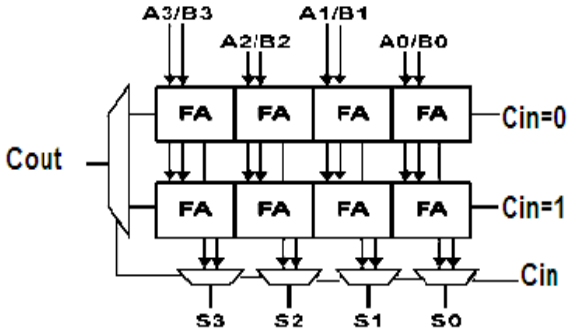

Fig.2. 4-Bit Carry Select Adder

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III. PROPOSED 16-BIT CARRY SELECT ADDER

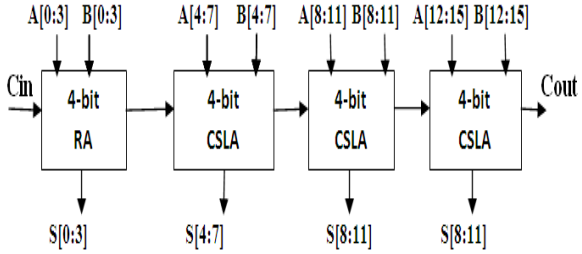

Fig.3. 16-Bit Carry Select Adder with Four 4-Bit Carry Select Adders

The above Figure 3 represents the proposed 16-bit carry select adder designed with four 4-bit carry select adders. Each 4-bit carry select adder is designed with eight transistor 1-bit full adder used for each full adder block in first RCA block with Cin = 0, a binary to excess-1 converter (BEC) instead of RCA with Cin = 1 in the regular csla and 2 transistor-multiplexers to achieve lower area and power consumption.

3.1. Basic 4-Bit CSLA Block Design

The basic adder block design using a ripple carry adder, BEC and multiplexer is explained in this section.

A. 8T Full Adder Circuit

The full adder function can be described as follows:

The addition of two 1-bit inputs a and b with forestage carry Cin calculates the two 1-bit outputs sum and Cout, where

$$Sum = a \oplus b \oplus Cin \quad \text{..... (1)}$$

$$Cout = a \cdot b + Cin \cdot (a \oplus b) \quad \text{..... (2)}$$

In our design, we rewrite the boolean function as

$$Sum = (a \oplus Cin) \cdot Cout + a \oplus Cin \quad \text{. ..... (3)}$$

$$Cout = (a \oplus Cin) \cdot b + a \oplus Cin \cdot a \quad \text{..... (4)}$$

From equations (3) and (4), the 8t-fulladder is designed as shown in figure.4.

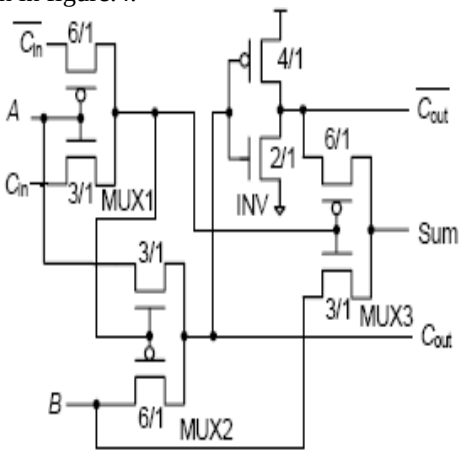

Fig.4. 8T-Full Adder Circuit

The entire design process can be divided into several steps as follows:

1. (a ⊕ cin)'or (a⊕cin) is needed as a control signal in multiplexers mux2 and mux3 to generate Cout and sum, in this circuit, a ⊕ Cin is implemented by mux1

2. The multiplexer circuit mux2 is adopted in our proposed design to generate Cout followed by an inverter-inv. The inverter has three advantages for the circuit firstly, it speeds up the carry propagation as a buffer along the carry chain. Secondly, it provides complementary signals needed for the generation of sum. Thirdly, the inverter can improve the output voltage swing as a level restoring circuit.

3. The sum is generated by the multiplexer mux3 passing either b or Cout' according to the value of a ⊕ Cin. The full adder circuit, which uses three multiplexers and an inverter, requires eight transistors. Choosing appropriate width to length ratios of transistors the W/L ratio, improves the threshold drop of the circuit the multiplexer uses transistor sizes of (W/L)p=6/1 and (W/L)n=3/1 for Pmos and Nmos, respectively, while the inverter uses the typical sizes of (W/L)p=4/1 and (W/L)n=2/1 .

B. Binary to excess-1 converter (BEC)

The basic work is to use binary to excess-1 converter (BEC) in the regular CSLA to achieve lower area and increased speed of operation. This logic is replaced in RCA with Cin=1.This logic can be implemented for different bits which are used in the modified design. The main advantage of this BEC logic comes from the fact that it uses lesser number of logic gates than the n-bit full adder (FA) structure. As stated above the main idea of this work is to use BEC instead of the RCA with Cin=1 in order to reduce the area and increase the speed of operation in the regular CSLA to obtain modified CSLA. To replace the n-bit RCA, an n+1-bit BEC logic is required. The structure and the function table of a 4-bit BEC are shown in figure 5 and table 1, respectively.

Table 1: Function Table of the 4-Bit BEC

Binary Input [3:0]	One bit excess X[3:0]
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

The boolean expressions of the 4-bit BEC is listed as below is obtained by using k-map solution method. (Note the functional symbols as ~ not, & and, ^ xor).

X0 = ~B0
X1 = B0 ^B1
X2 = B2 ^ (B0 & B1)
X3 = B3 ^ (B0 & B1 & B2)

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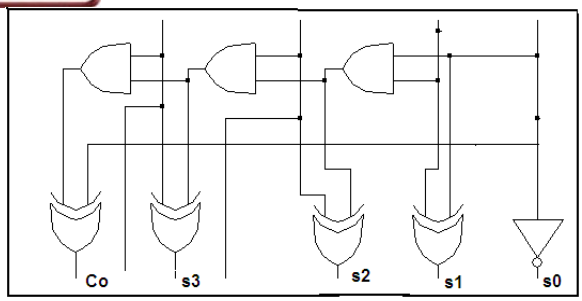

Fig.5. Binary to Excess-1 Converter (4-Bit BEC)

C. 2-TRANSISTOR MULTIPLEXER CELL

Figure 6 shows the implementation of multiplexer to select correct carry output based on carry input available as carry out from the previous block. It is implemented in pass transistor logic since pass transistor passes good '0', but a bad '1', the inverter has also been inversely rationed to provide faster 1 to 0 transitions.

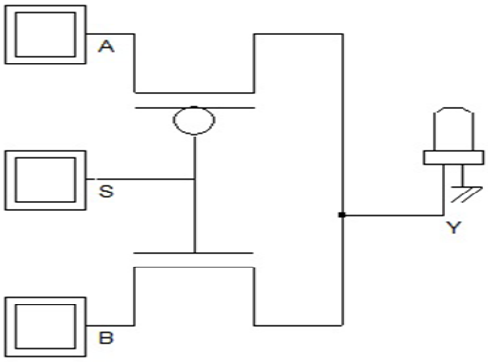

Fig.6. 2-Transistor Multiplexer Cell

IV. RESULT ANALYSIS

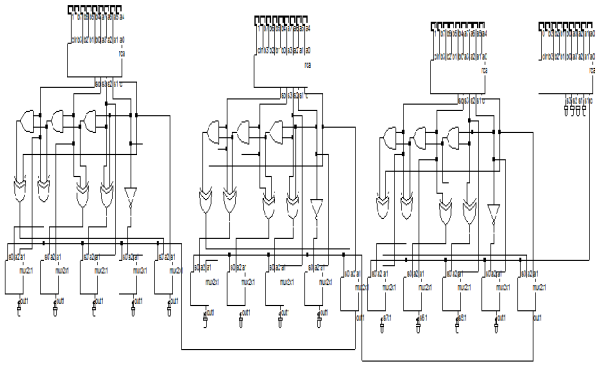

Fig.7. Schematic of 16-Bit Carry Select Adder with Four 4-Bit Carry Select Adders

The above Figure 7 shows schematic of 16-bit carry select adder with three 4-bit carry select adders and one 4-bit ripple carry adder. The schematic is obtained by designing with DSCH 2.6c tool. Table 2 illustrates power area and delay of existing CSLA and also the proposed CSLA. For the analysis of power, area & delay MICROWIND tool is used. Table 2 shows that power consumption is reduced by around 15% compared to regular CSLA. Similarly in proposed CSLA area is also reduced by around 55%.Delay in proposed CSLA is increased compared with existing CSLA.

Table 2 : Performance Parameters

Parameters	Existing CSLA	Proposed CSLA
Power(mw)	17.2	14.8
Area(mm2)	13616	6182
Delay(ns)	6.02	16.01

V. CONCLUSION

An efficient approach is proposed in this paper to reduce the area and power in the 16-bit CSLA design. Using of eight transistor full adder block in first RCA block with Cin= 0 reduce area and power consumption. The reduction in the number of gates is obtained by simply replacing the RCA with Cin input as one with BEC in the structure. The reduced number of gates of this work offers the great advantage in the reduction of area by 55% and also the total power by15%.The modified CSLA architecture is therefore, low area, low power, and with slight increase in delay is simple and efficient for VLSI hardware implementation.

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